Amendments to the Specification

Please replace the paragraph running from line 9 on page 4 through line 10 on page 5 with the following amended paragraph:

The method of fabricating a MOSFET device wherein the definition of an insulator offset spacer located on the sides of a conductive gate structure, and the removal of unwanted portions of a high-k gate insulator layer, both accomplished via a single dry etch procedure, will now be described in detail. Semiconductor substrate 1, comprised of P type single crystalline silicon featuring a <100> crystallographic orientation, is used and schematically shown in Fig. 1. Isolation regions, not shown in the drawings, are formed in top portions of non-device regions of semiconductor substrate 1. Isolation regions can be either thermally oxidized field oxide (FOX) regions, or insulator filled shallow trench isolation (STI) regions. Attempts to maximize device performance can be directed to numerous components of a device. For example MOSFET device performance can be increased with decreasing gate insulator thickness. However gate insulator layers comprised of silicon dioxide with a dielectric constant of about 3.9, can present leakage problems when used with thicknesses of less than 10 Angstroms. The ability to use a material for the gate insulator layer comprised with a dielectric constant greater than that of silicon dioxide allows the use of thinner gate insulator layers with less risk of leakage when compared to silicon dioxide counterparts of the same thickness. Therefore to reduce the risk of leakage a thin dielectric layer with a high dielectric constant will be used for the gate insulator layer. Insulator layer 2, comprised with a high dielectric constant (high-k) is next formed on semiconductor substrate 1. High-k layer 2, can be comprised of silicon nitride, tantalum oxide, silicon oxynitride, zirconium oxide, hafnium oxide, or aluminum oxide, ~~and silicon oxide,~~ featuring a dielectric constant greater than 4. High-k layer 2, shown schematically in Fig. 1, is formed at a thickness between about 10 to 200 Angstroms, via chemical vapor deposition (CVD) procedures.